

CLAIMS

Please amend the claims as follows.

1. (Original) A semiconductor integrated circuit comprising:
a plurality of data output pins;
a data processing circuit to generate output signals responsive to an input signal; and
an output selection circuit with at least a normal mode and a test mode;
where a first group of output signals are provided to a first group of data output pins in a first test cycle of the test mode; and
where a second group of output signals are provided to a second group of data output pins during a second test cycle of the test mode.
2. (Original) The semiconductor integrated circuit of claim 1 where the output selection circuit repeats the first and second test cycles during testing.
3. (Currently amended) The semiconductor integrated circuit of claim 1
where the output selection circuit sends ~~i th-odd~~ output signals (~~i being a positive integer~~)
to ~~i th-odd~~ data output pins during the first cycle of the test mode; and
where the output selection circuit sends ~~$(i+1)$ th-even~~ output signals to ~~i th-even~~ output pins during the second test cycle of the test mode.
4. (Currently amended) The semiconductor integrated circuit of claim 1
where the output selection circuit sends ~~i th-odd~~ output signals (~~i being a positive integer~~)
to ~~$(i+1)$ th-even~~ data output pins during the first cycle of the test mode; and
where the output selection circuit sends ~~the $(i+1)$ th-even~~ output signals to ~~$(i+1)$ th-odd~~ output pins during the second test cycle of the test mode.
5. (Canceled)
6. (Canceled)

7. (Currently amended) A method for outputting data during a test mode of a semiconductor integrated circuit having a plurality of data output pins, the method comprising:
sending some output signals to a first group of the data output pins during a first phase of the test mode; and
sending remaining output signals to the first group of the data output pins during the second phase of the test mode.
8. (Currently amended) The method of claim 7 where the sending some output signals and the sending remaining output signals are repeated during [[a]]the test mode.
9. (Original) The method of claim 7 where sending some output signals includes sending i th output signals (i being a positive integer) are sent to i th data output pins.
10. (Original) The method of claim 9 where i is a positive odd integer.
11. (Original) The method of claim 7 where sending remaining output signals includes sending $(i+1)$ th output signals (i being a positive integer) to i th data output pins.
12. (Canceled)
13. (Canceled)
14. (Canceled)
15. (Canceled)
16. (New) The semiconductor integrated circuit of claim 1 where the output selection circuit is adapted to send all output signals to corresponding output pins during the normal mode.
17. (New) The method of claim 7 where i is a positive even integer.